UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. | |
|----------------------------|---|----------------------|---------------------|------------------|--|
| 10/574,065 | 10/574,065 03/30/2006 Theodore J. Letavic | | | 9391 | |
| 65913 NXP , B.V. | 7590 02/18/200 | EXAMINER | | | |
| NXP INTELLE | ECTUAL PROPERTY | HU, SHOUXIANG | | | |
| M/S41-SJ 1109 MCKAY | DRIVE | ART UNIT | PAPER NUMBER | | |
| SAN JOSE, CA | A 95131 | 2811 | | | |
| | | | | | |
| | | NOTIFICATION DATE | DELIVERY MODE | | |
| | | | 02/18/2009 | ELECTRONIC | |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

| | | 1 | Application No. | | Applicant(s) | | | | |
|---|--|--|--|--|--|-------------|--|--|--|
| | | | 10/574,065 | | LETAVIC, THEODORE J. | | | | |
| Office Action Summary | | E | Examiner | | Art Unit | | | | |
| | | | Shouxiang Hu | | 2811 | | | | |
| Period fo | The MAILING DATE of this commur or Reply | nication appea | ars on the cover sh | eet with the co | orrespondence ad | ddress | | | |
| WHIC - Exter after - If NC - Failu Any (| CRTENED STATUTORY PERIOD FOR CHEVER IS LONGER, FROM THE INSIDE STATUTORY PERIOD FOR CHEVER IS LONGER, FROM THE INSIDE STATE IN THE STATE OF THE STAT | MAILING DAT s of 37 CFR 1.136(in munication. tatutory period will a will, by statute, ca | TE OF THIS COMN a). In no event, however, apply and will expire SIX of the application to become | MUNICATION may a reply be time (6) MONTHS from the | l. ely filed he mailing date of this o) (35 U.S.C. § 133). | • | | | |
| Status | | | | | | | | | |
| 1) 又 | Responsive to communication(s) file | ed on <i>01 Dec</i> | ember 2008. | | | | | | |
| '= | | | ction is non-final. | | | | | | |
| 3) | Since this application is in condition | <i>,</i> — | | I matters, pro | secution as to the | e merits is | | | |
| - , | closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. | | | | | | | | |
| Dispositi | on of Claims | | | | | | | | |
| 4)🛛 | 4)⊠ Claim(s) <u>1-16</u> is/are pending in the application. | | | | | | | | |
| | 4a) Of the above claim(s) is/are withdrawn from consideration. | | | | | | | | |
| 5) | i) Claim(s) is/are allowed. | | | | | | | | |
| 6)⊠ | 6)⊠ Claim(s) <u>1-16</u> is/are rejected. | | | | | | | | |
| 7) | Claim(s) is/are objected to. | | | | | | | | |
| 8) | Claim(s) are subject to restri | ction and/or e | election requireme | nt. | | | | | |
| Applicati | on Papers | | | | | | | | |
| 9) | The specification is objected to by th | e Examiner. | | | | | | | |
| 10)⊠ The drawing(s) filed on <u>10 October 2008</u> is/are: a)□ accepted or b)⊠ objected to by the Examiner. | | | | | | | | | |
| | Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). | | | | | | | | |
| | Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). | | | | | | | | |
| 11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. | | | | | | | | | |
| Priority ι | ınder 35 U.S.C. § 119 | | | | | | | | |
| 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. | | | | | | | | | |
| 2) Notic 3) Inform | t(s) e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (I nation Disclosure Statement(s) (PTO/SB/08) r No(s)/Mail Date | PTO-948) | Pap 5) 🔲 Not | erview Summary (per No(s)/Mail Da ice of Informal Pa er: | te | | | | |

DETAILED ACTION

Drawings

1. The drawings were received on October 10, 2008. These drawings are disapproved.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the subject matters that the field plate is on the insulation layer which in turn is above the gate electrode and that the field plate is connected to the gate electrode as recited in claims 1 and 13 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

In addition, Figs. 1 and 2 are further objected to, for the following reasons:

In Fig. 1, numeral 34 which should refer to a drain region according to the instant specification apparently is wrongly pointed to a drain electrode that should be identified with numeral 44. In addition, the drain extension region 46 and the real drain region (34) are two regions with substantially different doping concentrations; but, the boundary between these two regions is missing in Fig. 1.

In addition, Figs. 1 and 2 include the following reference character(s) that is not mentioned in the description: "48".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

Application/Control Number: 10/574,065 Page 3

Art Unit: 2811

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

- 2. The following is a quotation of the first paragraph of 35 U.S.C. 112:
 - The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
- 3. Claims 1-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1 and 13 each recite the subject matters that the field plate is on the insulation layer which in turn is above the gate electrode and that the field plate is connected to the gate electrode. However, the disclosure lacks an adequate description regarding these subject matters. It is not clear where and/or how the gate electrode and the field plate could be connected together, given that the gate electrode and the field plate are formed of different layers with the recited insulation layer therebetween.

Claims 1-16 either directly recite (such as in claim 1) or intended to imply (such as in claim 13, as further evidenced in claim 14) the subject matter that the recited field plate is formed so as to form a linear lateral electric field distribution in the lateral drift region. However, such subject matter appears to be inconsistent with the fact that a (substantially) linear voltage/potential distribution across the field plate is naturally formed in the instant invention (see lines 7-14 on page 4 of the instant specification; as further evidenced in claims 11 and 13), given that: such linear voltage/potential distribution will inherently tend to cause the voltage/potential distribution in the nearby lateral drift region also to be linear; and the voltage (or potential) and the field cannot both be simultaneously linear in any region, which is because:

The field (E) is a derivative of the voltage (or potential; V), i.e., E = dV/dX. So, if V is linear (such as V = aX), the E has to be a constant (-a; a linear distribution is not always a constant). Or, if E is linear (such as E = bX), then V must be nonlinear (-0.5b X^2).

Accordingly, the subject matters as recited or implicated in the claims that recite the lateral electric field distribution in the lateral drift region can also be linear when the

Page 5

voltage/potential distribution across the nearby field plate is linear in the instant invention appear to be inconsistent with the general physics as provided above.

Claims 11 recites the subject matters that "said metallic regions in the field plate is connected to said source region and the remaining ones of said metallic regions are capacitively coupled to the first one of said metallic regions to linearly distribute a voltage at the source region across the field plate." However, the original disclosure lacks an adequate description regarding these subject matters, as it is not clear how the voltage at the source region across the field plate could be linearly distributed, given that there is a biasing voltage/potential of the gate electrode (36) on the path between the source region (28) and the field plate region (52b) and/or between the source region (28) and the drain region (34); and, such a biasing voltage/potential of the gate electrode (36) would naturally cause a nonlinear disturbance to the voltage at the source region across the field plate.

4. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 13 each recite the terms of lateral drift region, body region and drain region, but fail to clarify their definite positional relationship, as it is not clear: whether the lateral drift region and the body region are laterally side by side to each other and/or they vertically overlap with each other; and/or, whether the lateral drift

region and the drain region are laterally side by side to each other and/or they vertically overlap with each other.

In claim 3, the term of "said spacers" lacks a sufficient antecedent basis in the claim.

Claim 5 recites the term of "another dielectric layer", but fails to clarify its relationship with the "insulation layer" already defined in claim 1.

Claim Rejections - 35 USC § 103

- 5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 6. Claims 1-16, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as obvious over Letavic (Letavic et al., US 6,127,703) in view of Nakagawa (US 4,614,959; of record), or in the alternative, over Nakagawa in view of Letavic.

Letavic discloses a lateral thin-film Silicon-On-Insulator (SOI) device (Fig. 1), comprising: a semiconductor substrate (22), a buried insulating layer (24) on said substrate, and a lateral MOS transistor device in an SOI layer (26) on said buried insulating layer and having a source region (28; such as p type) of a first type conductivity formed in a body region (30; such as n type) of a second type conductivity, a lateral drift region (32) of a second type conductivity adjacent said body region, a

Art Unit: 2811

drain region (34) of said first type conductivity and laterally spaced apart from said body region by the lateral drift region; a gate electrode (36) insulated from said body region and drift region by an insulation region (an underlying portion of 38), an insulation lager (an upper portion of 38) on and laterally adjacent to the gate electrode.

Although Letavic does not expressly disclose that the device can further include a field plate comprising a first layer having plural laterally separated metallic regions, one of ordinary skill in the art would readily recognize that such field plate can be desirably formed so as to improve high voltage performance, as evidenced in Nakagawa (Fig. 10). In Nakagawa, the field plate (6', 13', 7') is on the insulation layer (8') and is connected to the source region and extending substantially over the surface of the substrate, wherein such field plate comprises a first layer of plural metallic regions (6', 13', 7') which are isolated laterally from one another by substantially same-sized spaces (filled with portions of the dielectric layer 8"), thus voltage (or potential) distribution across the field plate (from the end pieces 6' to the end piece 7') is inherently substantially linear, in a manner substantially same as that in the instant invention.

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the field plate of Nakagawa into the device of Letavic, so that a device with improved high voltage performance would be obtained.

Or, in the alternative, it would also have been obvious to one of the ordinary skill in the art at the time the invention was made to incorporate the SOI-based device

structure of Letavic into the device of Nakagawa, so that a high voltage device on desired SOI substrate would be obtained.

And, with the above field plate being formed in the above collectively taught device, the electric field in the underlying and nearby lateral drift region therein would have a lateral distribution that would be naturally substantially same as whatever the distribution is in the instant invention, since the spaces that laterally separate the plural metallic regions in the first layer of the above field plate are substantially same in size, inherently causing the voltage (or potential) distribution across the field plate (from the end pieces 6' to the end piece 7') to be substantially linear, in a manner substantially same as that in the instant invention.

Regarding claims 3-5, it is further noted that the field plate of Nakagawa further comprises another layer of plural metallic regions (12') located above the spaces between the metallic regions in the first layer, laterally isolated from one another, and isolated from the metallic regions of said first layer by the dielectric layer (8").

Regarding claims 4 and 5, it is further noted, it is art known that the dielectric layer can be formed of a silicon-rich nitride layer as to increase the breakdown voltage, as readily evidenced in the prior art such as William (William et al., US 5,374,843; see col. 11, line 67, through col. 12, line 29).

Regarding claims 6-8 and 15, it is further noted that the drift region in the device of Letavic has the linearly-graded charge profile.

Art Unit: 2811

Regarding claim 10, it is further noted that it is art known that the polarity of a semiconductor device can be readily reversed so as to obtained a device with desired opposite polarity.

Response to Arguments

7. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.

Application/Control Number: 10/574,065 Page 10

Art Unit: 2811

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/ Primary Examiner, Art Unit 2811